Class	Subclass

ISSUE CLASSIFICATION

09/652550

C

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED 6/07 Q.A. 1C	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/652550		257~~436~~	296 ~~310~~	2811	Q. Vu

APPLICANTS

Keiji Jono
Hirokazu Ueda
Hiroyuki Watanabe

TITLE

Methods of forming an isolation trench in a semiconductor, methods of forming an isolation trench in a surface of a silicon wafer, methods of forming an isolation trench-isolated transistor, trench-isolated transistor, trench isolation structures formed

PTO-2040 11/2000

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
☒ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.				ISSUE BATCH NUMBER	

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

WARNING:

The information disclosed herein may be restricted. Unauthorized disclosure may be prohibited by the United States Code Title 35, Sections 122, 181 and 368. Possession outside the U.S. Patent & Trademark Office is restricted to authorized employees and contractors only.

Form PTO-436A (Rev. 6/99)

FILED WITH: ☐ DISK (CRF) ☐ FICHE ☐ CD-ROM

(Attached in pocket on right inside flap)

(FACE)